DIGITAL SIGNAL PROCESSOR CONTROL ALGORITHM FOR PWM INVERTER

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ABSTRACT

Recent developments in power electronic device technology promises faster switching capability at high power. The hybrid pulse width modulation method which requires two of the four switches in a full bridge inverter are used, and enable pulse pattern operation at high frequency. The use of two level switching instead of three level switching enables the use of higher frequency for given computation time delay. The proposed control scheme is implemented using bi-polar junction transistors (BJT) controlling an inverter to produce a very low frequency (THD) sinusoidal output voltage. Simulation and experimental results are presented to verify the performance.

1 INTRODUCTION

The full bridge inverter in Fig. (1) is widely employed in various applications such as motor drives and active filter [1][2].

The inverter comprises switching poles S1, S2, S3, S4, S5 and S6. The switching poles are commonly controlled by a variety of PWM techniques [3], and by pulse-shifted square-wave drives [4]. Application of switching devices such as IGBT achieve very high switching frequency PWM inverters with improved performance [5]. With the availability of high frequency switching devices the instantaneous feedback control (IFC) was presented [6]. The advantages of this technique are high transient response and the disadvantage is that relatively large harmonic amplitudes occur for frequencies near the average switching frequency.

By using a microprocessor, a digital feedback approach such as a microprocessor deadbeat control was proposed [7][8]. The PWM inverter system is converted into a discrete time system and a state feedback output deadbeat control is applied.

Manuscript received from Dr; A. A. Heggo on : 11/11/1998
Accepted on: 13/6/1999
Engineering Research Bulletin, Vol 22,No 3, 1999
Minufiya University, Faculty of Engineering , Shebin El-Kom , Egypt, ISSN 1110-1180

Digital signal processor (DSPs) are now applied for the control of power electronics and drive systems. DSPs are much faster (ten or one hundred times) than a microprocessor [9]. Simplification of control hardware and corresponding reduction of cost are the principal advantages of DSP control [10].

A digital controller was used to implement the control algorithm and provide switching signal to the power circuit. The proposed control model is implemented using DSPs controlling an inverter to produce a very low total harmonic distortion (THD) in sinusoidal output voltage.

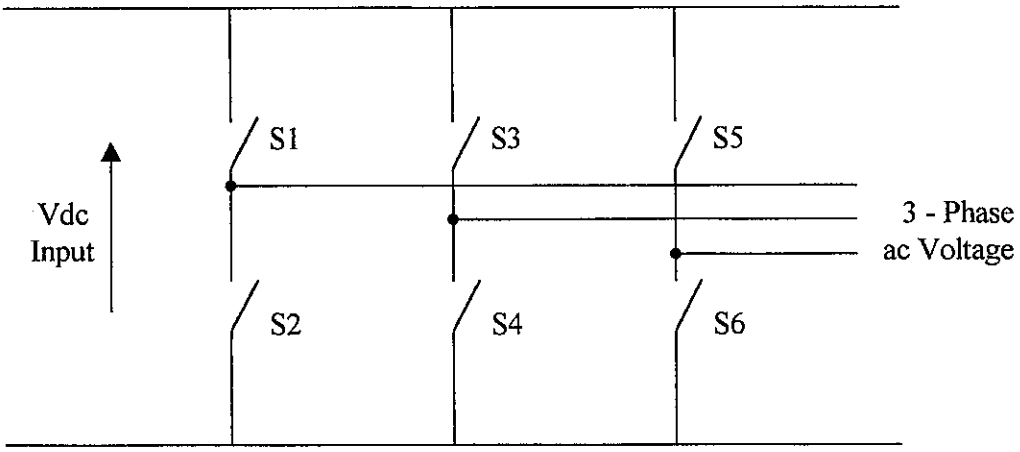

Fig. 1 - System description

2 CONTROL ALGORITHM

A modified algorithm of the deadbeat controlled PWM inverter is suitable for stabilised power supply systems. Two levels are used in the pulse pattern. Given a computation time delay, twice the switching frequency can be adapted resulting in lower THD sinusoidal output. This work presents the deduction of a new discrete time state equation and the proposed deadbeat control algorithm for PWM inverters. Simulation results are obtained and presented.

2.1 Deadbeat Control

This technique depends upon the digital feedback closed loop. This means measuring of output, and controls the inverter switches to generate the required PWM pattern to produce a low THD sinusoidal output voltage.

The digital control algorithm is designed to control pulse width such that the output voltage equals the sinusoidal reference at every sampling instant, Fig. (2).

So the output voltage will be in phase and very close to sinusoidal reference. Any deviation of the output voltage from the reference due to a load disturbance or non-linear circuits is controlled within one sampling interval Ts.

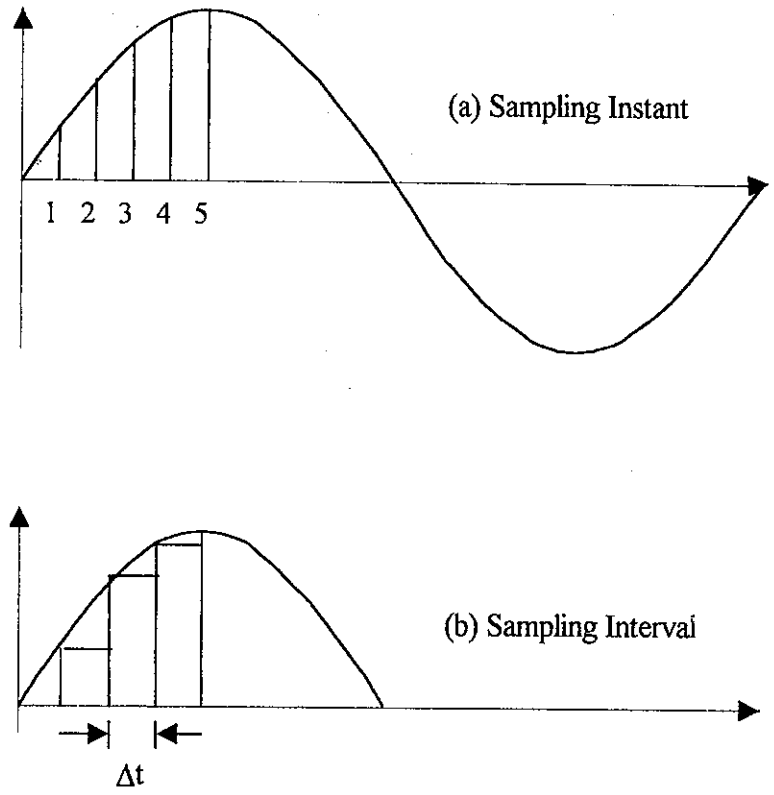

Fig. 2 - Sampling Time

The PWM pattern is determined at every sampling instant digitally by DSPs based on the output measurements and the references.

2.2 State Model

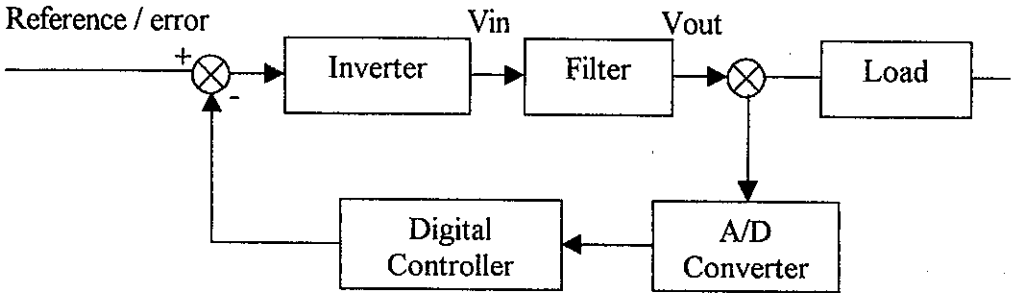

Fig. 3 - Block Diagram of Digital Control Inverter

As shown in Fig. (3) the deadbeat controller for PWM inverter is considered. The inverter, L-C filter and resistive load represent the plant of closed loop digital feedback system.

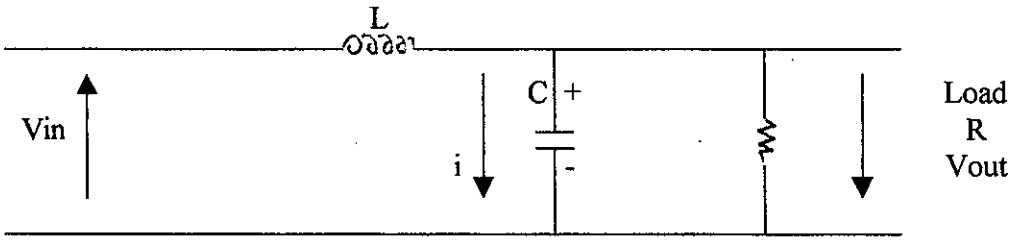

Fig. 4 - State Model

The circuit shown in Fig. (4) is modelled as a second-order system with state vector *[V,i]*, where *V* is load voltage and *i* is capacitor current.

The state equation becomes:

$$\begin{bmatrix} V' \\ i' \end{bmatrix} = A.\begin{bmatrix} V \\ i \end{bmatrix} + B.V_{in} \tag{1}$$

where:

$$A = \begin{bmatrix} 0 & \frac{1}{c} \\ \frac{-1}{L} & \frac{-1}{Rc} \end{bmatrix} \text{ and } B = \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} \tag{2}$$

2.3 Two Level scheme

The basic circuit for the deadbeat controlled PWM inverter with a two level switching pattern is shown in Fig. (5).

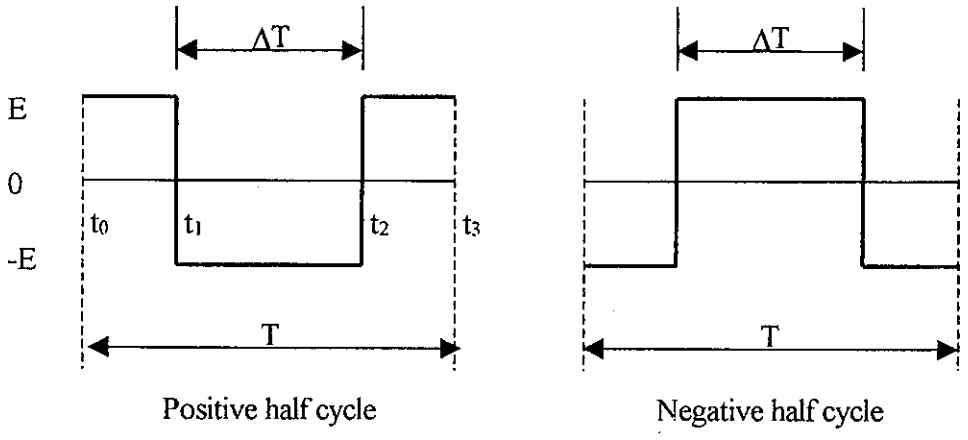

Fig. 5 - Two Level Deadbeat Controlled PWM Inverter Pattern

The continuous time domain state (1) can be written as:

$$\dot{x} = Ax + Bu \tag{3}$$

where:

x = state vector
u = scalar input
A = non-singular matrix

Then the closed form circuit is:

$$x(t) = e^{A(t-t_0)}x(t_0) + \int_{t_0}^{t} Ae^{A(t-c)}Bu(\tau)d\tau \tag{4}$$

where $x(t_o)$ is the initial state vector at $t = t_o$ if the input u is constant for $t_o \leq t \leq t_1$

then Eq.(4) becomes:

$$x(t_1) = e^{A(t-t_0)}x(t_0) + A^{-1}\left(e^{A(t_1-t_0)} - 1\right. \tag{5}$$

using Eq.(5), the discrete-time system equation with the input is derived as follows:

a) For $t_o < t < t_1$ and $E = u$

$$x(t_1) = e^{A(t_1-t_0)}x(t_0) + A^{-1}(e^{A(T-\Delta T)} - 1)BE \tag{6}$$

For $t_1 < t < t_2$ and $-E = u$

$$x(t_2) = e^{A(t_2-t_0)}x(t_0) + e^{A\Delta T}A^{-1}(e^{A(T-\Delta T)/2} - 1)BE \tag{7}$$

For $t_2 < t < t_3$ and $E = u$

$$\begin{aligned} x(t_3) = \; & e^{AT}x(t_0) + e^{A(T-\Delta T)/2}e^{AT}A^{-1}(e^{A(T-\Delta T)/2} - 1)BE \\ & - e^{A(T-\Delta T)/2}A^{-1}(e^{AT} - 1)BE + A^{-1}(e^{A(t-\Delta T)/2} - 1)BE \end{aligned} \tag{8}$$

and by expansion the terms:

$A\Delta T/2$

$$e \approx 1 + \frac{A\Delta T}{2} + \frac{A^2(\Delta T/2)^2}{2} \tag{9}$$

$$e^{AT} \approx 1 + AT + \frac{(AT)^2}{2} \tag{10}$$

then Eq.(8) becomes:

$$x[(K+1)T] = e^{AT}x(KT) - 2e^{AT/2}BE\Delta T + (\frac{T + AT^2}{2} + \frac{A^2T^3}{6})BE \tag{11}$$

where $(K + 1) = t_3$ and $KT = t_o$

this is a discrete-time system of Eq.(3)

Rewriting Eq.(11) gives:

$$\begin{bmatrix} V(K+1) \\ i(K+1) \end{bmatrix} = \begin{bmatrix} f_{11} & f_{12} \\ f_{21} & f_{22} \end{bmatrix} \tag{12}$$

where:

f_{ij} is corresponding to element of e^{AT}

g_i is corresponding to element of $2e^{AT/2}BE$

h_i is corresponding to element of $(T + AT^2/2 + AT^3/6)BE$

$V(K)$, $i(K)$ and $\Delta T(K)$ represent the values of voltage, the current and the sampling time:

$t = KT$

Therefore, by analysis of Eq.(12) gives:

$$V(K+1) = f_{11}V(K) + f_{12}i(K) - g_1\Delta T(K) + h_1 \tag{13}$$

$$i(K+1) = f_{21}(VK) + f_{22}(i(K)) - g_2\Delta T(K) + h_2 \tag{14}$$

3 COMPUTER SIMULATION

The following circuit parameters were used in computing the pulse width $\Delta T(K)$,

and to obtain waveforms of voltage and current.

E = 375 V
R = 2 KΩ
L = 11 mH
c = 100 μF
N = 75
T = 266 μs

Scheme / Load	Line Load
Two level scheme THD/fundamental	0.889/15.6

The simulation results are shown in Figs. (6), (7) and (8)

4 CONCLUSION

A two deadbeat controller is used to minimise the total harmonic distribution of the digital inverter. This scheme will lead to the following advantages:

- provide more computation time for the same interval switching number
- provide a maximum voltage equal to the dc busbar voltage during each switching interval, $E_i + E$

The obtained results show the waveforms of output voltages during various types of modulation.

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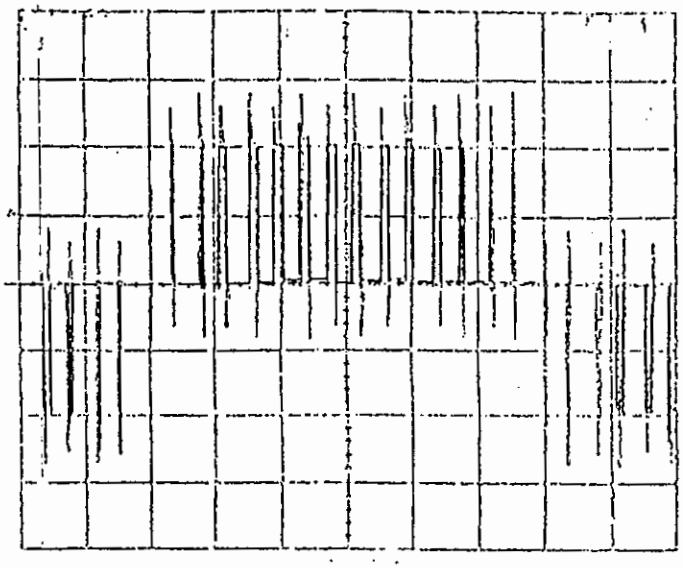
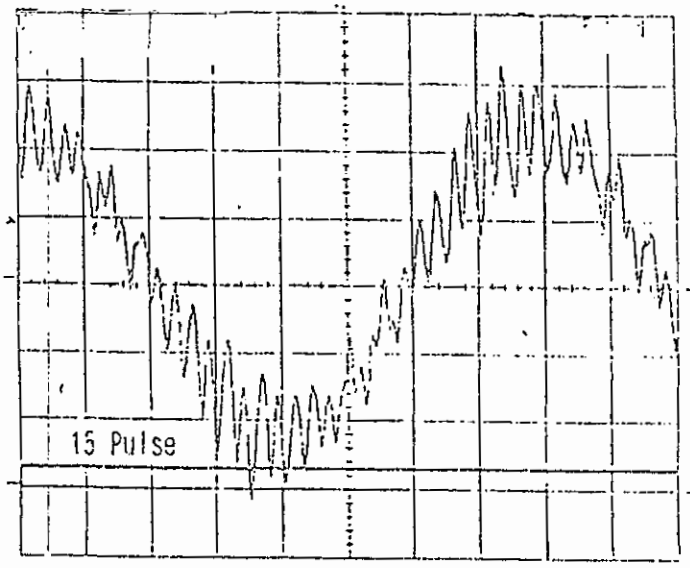
6 NOMENCLATURE

ΔT	sampling time
A, B	matrix of state variable equation
A/D	analogue / digital converter
C	filter capacitance
DSP	digital signal processor
f	output frequency
i	capacitor current
K	integer, positive number 0, 1, 2, 3
L	filter inductive
N	no. of sampling
PWM	pulse width modulation
R	load resistance
T	interval time
V	load output voltage
V_{in}	input voltage

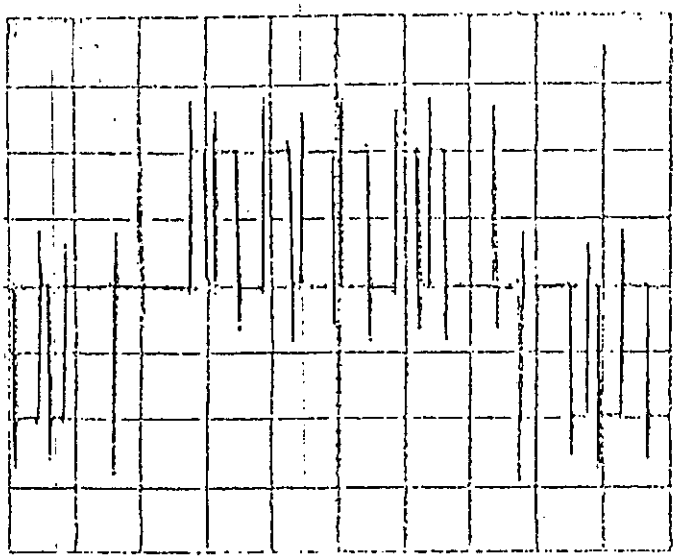


(a) VOLTAGE WAVEFORM

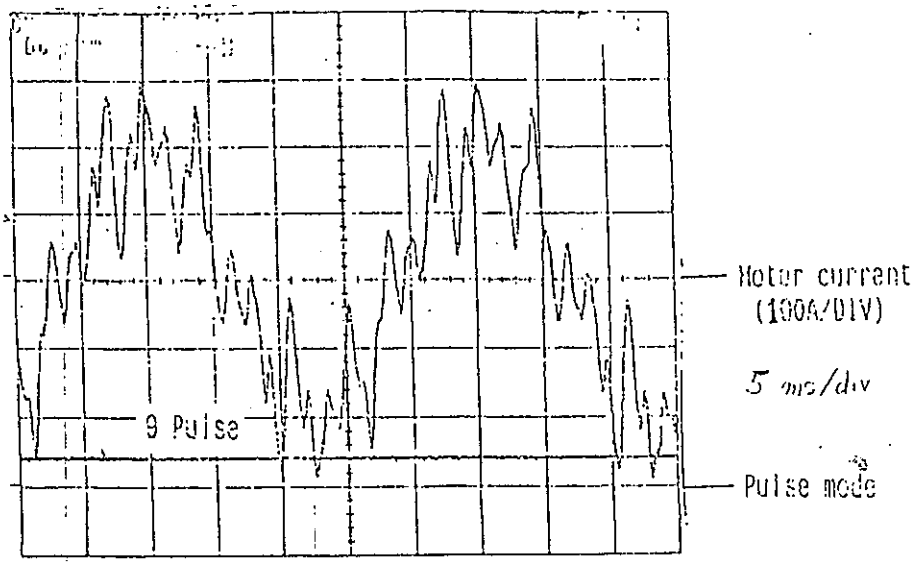


(b) CURRENT WAVEFORM

Fig.6 The voltage and current wavetorms under the "15 Pulse Modulation Mode"

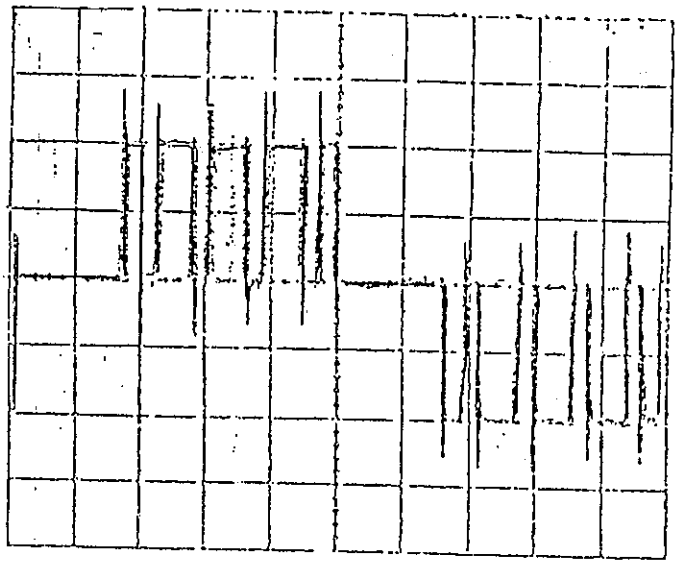


(7-a) VOLTAGE WAVEFORM

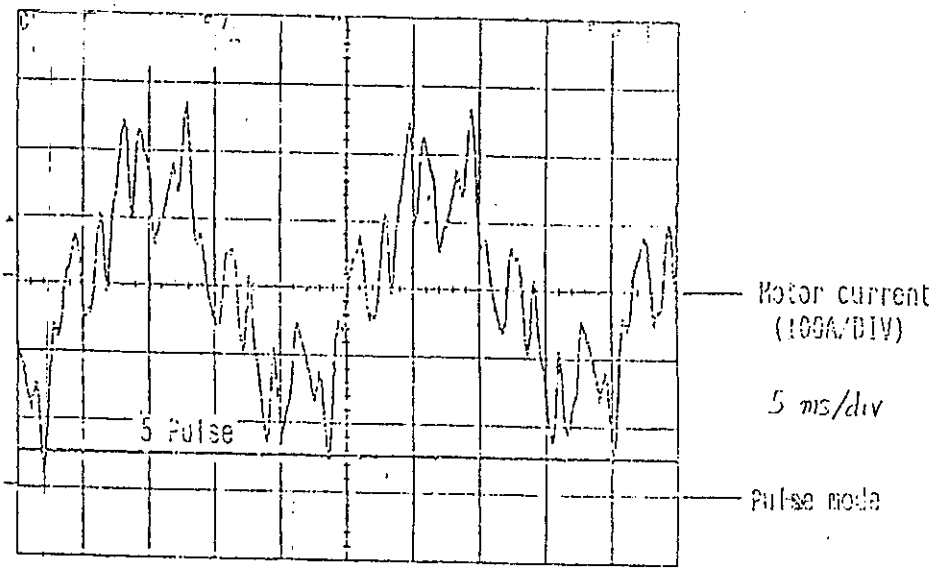


(7-b) CURRENT WAVEFORM

Fig.7 The voltage and current waveforms under the "9 Pulse Modulation Mode"



(a) VOLTAGE WAVEFORM



(b) CURRENT WAVEFORM

Fig.8 The voltage and current waveforms under the "5 Pulse Modulation Mode"

التحكم اللوغارتمى بمعالج الإشارة الرقمى
لمحول تعديل إتساع النبضة .

الملخص :-

إن التقدم الحديث فى تكنولوجيا أجهزة إليكترونيات القوى إتاح سرعة إمكانية إستخدام الدوائر الكهربية عند القدرات العا!.ية إن طريقة تعديل إتساع النهضة لمهجن تتطلب إستخدام مفتاحين من أربعة فقط فى حالة محول القنطرة الكامل وبذا نحصل على كفاءة عاليه . وإستخدام مستويين للفصل والتوصيل بدلاً من ثلاثة مستويات يمكن من العمل بترددات أعلى لنفس التأخيـــر الزمنى . وفى هذا النموذج المقدم ثم إستخدام ترانز – سطور الوصلة القطبية للتحكم فى المحول لإنتاج موجة جنية يصاحبها أقل قدر من التوافقيات المشوهة . وتم الحصول على نتائـــــج المحاكاه وتم التعليق عليها لإثبات خواص الدائرة .