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A Proposed Five-level Neutral Point Clamped Inverter

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ABSTRACT
This paper presents a proposed five-level inverter based on conventional five-level Neutral Point Clamped (NPC) topology which is a type of Multilevel Inverters (MLIs). MLI is a great solution for high power application in addition to medium power, low power and renewable energy applications. The proposed topology reduces the number of input DC sources as compared with the conventional five level NPC topology. Also, this circuit reduces the conduction losses by reducing number of switches that turned on in each mode. The circuit operation analysis in each mode is illustrated. A proper modulation strategy based on Pulse Width Modulation PWM is applied on the proposed circuit. The simulation of the proposed circuit is carried out in MATLAB/SIMULINK environment. The results show a comparison between conventional five-level NPC and modified circuits which illustrate a good performance for the proposed one which make it suitable for many applications such as photovoltaic systems.

Keywords: *Five level inverter, NPC, multicarrier PWM technique, THD, conduction losses.*

1. Introduction

Multilevel Inverters (MLIs) have a great attention in industry in recent years because they are considered a solution for high power application such as large motor drives [1, 2] and High Voltage DC (HVDC) systems [3]. They are also applied in medium and low power application such as distributed power systems [1], photovoltaic systems [4] and voltage sag compensation [5]. The main concept of MLIs is to utilize isolated dc sources or a bank of series capacitors to generate ac voltage waveforms with higher amplitude and near sinusoidal waveform [6]. MLIs utilizes a high number of semiconductor switches, but due to their advantages, they still have a great attention [7-9].

The main advantages of MLIs are [10] low Total Harmonic (THD) of the output voltage due to multiple levels of waveform, low dv/dt of switches, low switching frequency which lead to reduction in switching losses, utilization of switches with lower voltage rating to obtain higher output voltage, reduce size of output filter, lower electromagnetic interference (EMI) and transformerless implementation. Although, MLIs have some drawbacks such as requirement of large number of power semiconductor switches and need to separate gate drive circuit for each switch which make the overall system more complex and expensive. There are three main conventional types of MLIs: Diode-clamped MLI (DCMLI) which also called Neutral Point Clamped (NPC) [11, 12], Flying Capacitor MLI (FCMLI) [1] and Cascaded H-bridge MLI (CHBMLI) [13, 14].

Neutral Point Clamped MLI was first proposed in 1981 as a three level inverter [11]. In this topology, only one DC source is needed and capacitors are utilized to split the DC voltage and provide a neutral point. The number of capacitors required is (N-1) where N is number of levels of output voltage. The power switches are connected in series with each other and their number equal 2(N-1). The clamping diodes are used to block the current and their number is (N-1)*(N-2). For example, Fig. 1 shows a power circuit for five-level NPC inverter. It consists of 8 switches, 6 diodes, 4 capacitors and one DC voltage source. The levels of output voltage are $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$, $-V_{dc}/2$. Although this topology uses only one DC voltage source, the voltages across the capacitors are unbalanced. To solve this problem, a balancing circuit is needed or a control method can be implemented which make the overall system more complex.

Flying-Capacitor MLI topology also called capacitor-clamped inverter. It is similar to NPCMLI with replacing the clamping diodes with clamping capacitors [1]. The number of power switches and DC-bus capacitors are the same as NPC topology but the number of clamping capacitors equal (N-1)*(N-2)/2. The function of clamping capacitors is generating the output voltages with its desired value.

This topology also needs only one DC voltage source. Fig. 2 shows five-level FC inverter. It consists of 8 switches, 4 DC-bus capacitors, 6 clamping capacitors and only one DC voltage source. The levels of output voltage are $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$, $-V_{dc}/2$. As the number of levels increase, the waveform of output voltage approaches from sinusoidal waveform.

Cascaded H-Bridge MLI inverter consist of a number of H-Bridge or Full-bridge cells which connected in series with each other with separate DC voltage sources [13]. DC voltage sources may be symmetrical or unsymmetrical. Fig. 3 shows the conventional circuit of five-level CHB inverter. It consists of two full-bridge cells and two DC voltage sources. The levels of output voltage are $+V_{dc1}$, $-V_{dc1}$, 0, $+V_{dc2}$, $-V_{dc2}$. The number of output voltage levels can be given by N= (m+2)/2 where m is the number of power switches. This topology has some advantages over NPCMLI and FCMLI such as it doesn't require clamping diodes and flying capacitors. Also, it doesn't have the problem of capacitor voltage unbalance.

Other topologies of MLIs have been proposed to increase number of levels of output voltage with reducing cost and size either by proposing configuration of topology or by modulation strategy. MLIs can be classified into two main categories according to their construction properties [15]: Single DC-voltage source inverter such as NPCMLI and FCMLI and Multi DC-voltage sources inverter which is divided into symmetrical and nonsymmetrical topologies such as CHBMLI.

This paper presents a proposed 5-level MLI with multicarrier Pulse Width Modulation PWM technique. The proposed topology provides some advantages over the conventional five level NPC topology such as reducing number of split capacitors and reducing number of switches that turning on in every mode and that reduces conduction losses.

This paper is organized as follows. Section 2 describes the construction of proposed five-level topology, its principle of operation and its modulation strategy. Section 3 presents the simulation results on Matlab/Simulink for proposed and conventional topologies. Section 4 presents the conclusion.

2. Configuration of Proposed Five-Level Topology

The construction of the proposed five-level topology is shown in Fig. 4. It consists of 8 switches, 4 diodes and 2 DC sources each one of value Vdc. Two DC voltage source are utilized instead of using one DC source and two DC-bus capacitors to avoid the problem of capacitor voltage unbalance. This topology can produce five levels of voltage +2Vdc, +Vdc, 0, -Vdc, -2Vdc. The function of diodes is to prevent current from flowing in the antiparallel diodes of IGBT's switches.

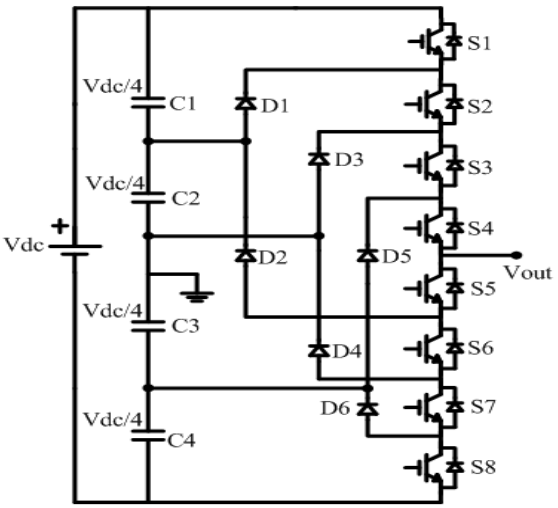


Fig. 1 Five-level NPC inverter

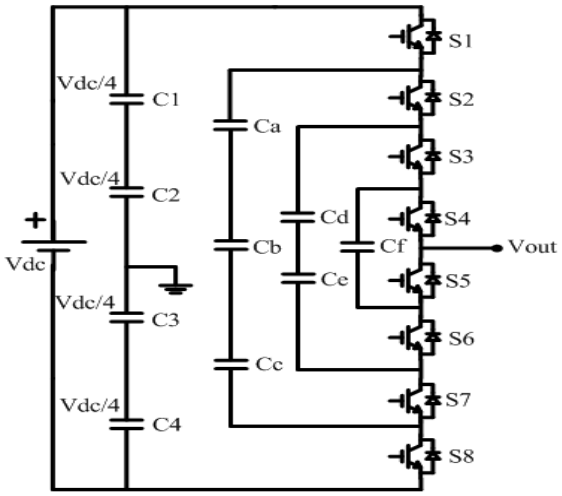


Fig. 2 Five-level FC inverter

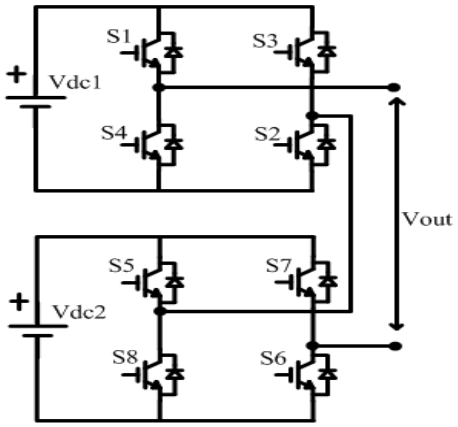


Fig. 3 Five-level CHB inverter

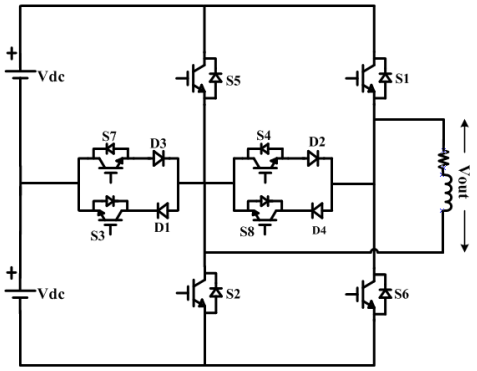


Fig. 4 Proposed Five-level topology

2.1 Principle of Operation

There are six modes of operation .Every mode is responsible for producing a certain level of voltage that is discussed in detail.

Mode(١)

-This mode is the active positive half cycle of load current as shown in Fig. 5(a). Switches S1 and S2 are turned on and all the other switches are turned off. The load current flows through S1, load and S2. The output voltage is equal to 2Vdc.

Vout = 2Vdc

Mode(٢)

- This mode is also in the active positive half cycle of load current as shown in Fig. 5(b). Switch S1 is keeping on in addition to turning on S3 and all the other switches are turned off. The current flows through S1, load, D1 and S3. The output voltage is equal to Vdc .

Vout = Vdc

Mode(٣)

- It is the freewheeling mode of the positive half cycle of load current as shown in Fig. 5(c). Switch S4 is on and all the other switches are turned off. The current flows through load, S4 and D2. The output voltage is equal to zero.

Vout = 0

Mode(٤)

- This is the active mode of the negative half cycle of load current as shown in Fig. 5(d). Switches S5 and S6 are turned on and all the other switches are turned off. The current flows through S5, load and S6. The output voltage equals -2Vdc.

Vout = -2Vdc

Mode (٥)

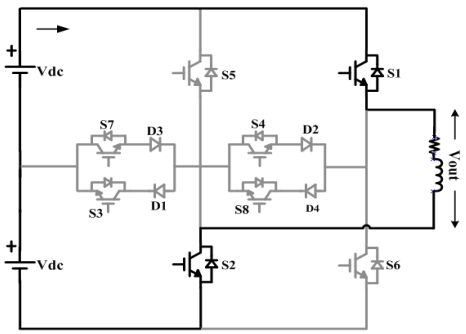
- It is also active mode in the negative half cycle of load current as shown in Fig. 5(e). Switch S6 is keeping on in addition to turning on S7 and all the other switches are turned off. The current flows through S7, D3, load and S6 producing output voltage equal to –Vdc.

Vout = -Vdc

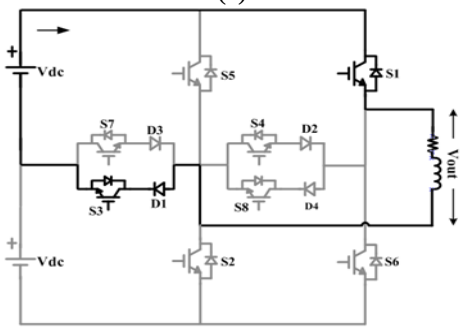
Mode(٦)

- This is the freewheeling mode in the negative half cycle as shown in Fig. 5(f). Switch S8 is switched on and all the other switches are turned off. Current flows through load, D4 and S8 producing output voltage equal to zero.

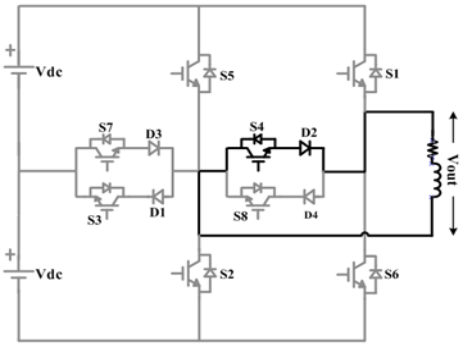
Vout = 0



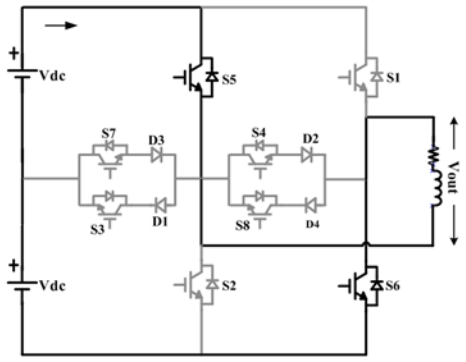
(a)



(b)



(c)



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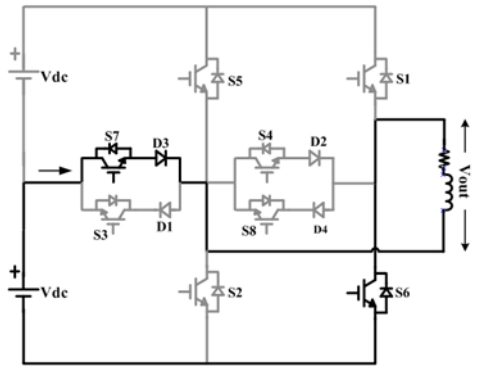

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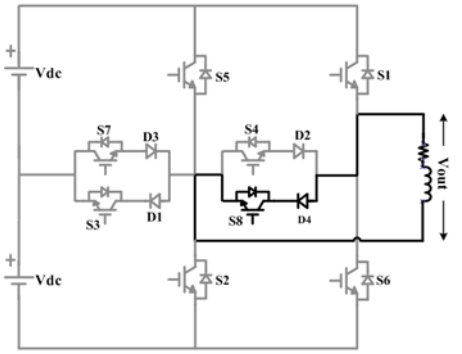


(f)

Fig. 5 Modes of operation a) Mode 1, Vout=+2Vdc b) Mode 2, Vout=+Vdc c) Mode 3, Vout=0 d) Mode 4, Vout=-2Vdc e) Mode 5, Vout=-Vdc f) Mode 6, Vout=0

2.2 Modulation Strategy and Switching Table

Table 1 shows the switching pattern through one cycle to obtain five levels of output voltage. The 1's represents the on-state and 0's represents the off-state. To control the output voltage of proposed topology, we can use multilevel modulation techniques which divided into two main groups based on the switching frequency used to drive switches of the inverter: a) Fundamental switching frequency and b) High switching frequency.

The second type also called Pulse Width Modulation PWM and common types of it are sinusoidal PWM, space vector PWM, multicarrier PWM and phase shifted PWM [6, 16]. Multicarrier PWM is chosen to generate suitable gating signals. Number of carriers depends on number of levels of voltage (N) that is equal to (N-1). So, number of carriers here equal to 4 signals with same amplitude and same frequency but different offset voltage. Fig. 6 shows the method of producing switching pulses using multicarrier PWM and the switching pattern. The four carriers are compared to reference waveform to produce switching pulses.

Table 1- Switching table of proposed topology

	S1	S2	S3	S4	S5	S6	S7	S8
+2Vdc	1	1	0	0	0	0	0	0
+Vdc	1	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	1
-2Vdc	0	0	0	0	1	1	0	0
-Vdc	0	0	1	0	0	1	1	0
0	0	0	0	1	0	0	0	1

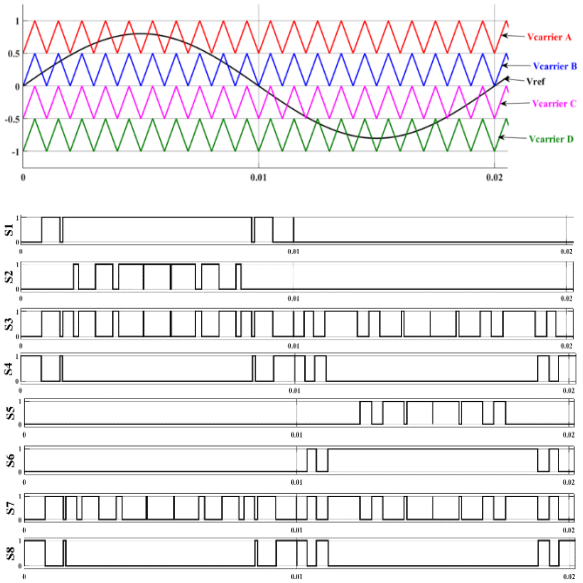
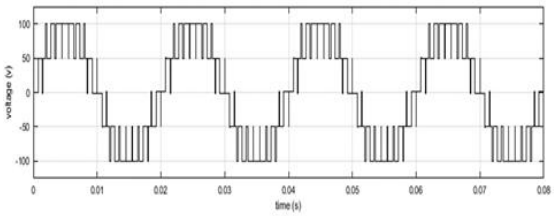


Fig. 6 PWM switching pattern of proposed topology

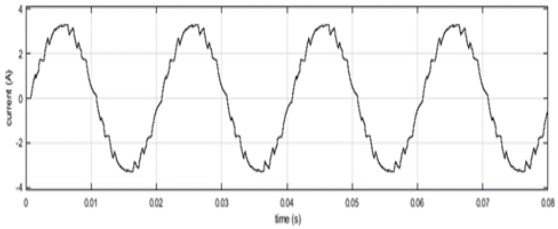
3. Simulation Results

To prove the validity of the proposed topology, a simulation model of single-phase five level inverter is built in Matlab/Simulink. Two DC sources are utilized in the proposed topology and four Dc sources in conventional topology with value of each one equal 50V. The frequency of all carriers is 1KHZ and the frequency of the reference signal is 50HZ. The output is shown in RL load with values of 20 Ω and 24 mH. Fig. 7 (a) and (b) shows the output voltage Vout and output current Iout of conventional NPC 5-level topology respectively. It is shown that the levels of Vout are +100V, +50V, 0, -100V, -50V. Fig. 8 (a) and (b) shows the harmonic spectrum waveform of the output voltage Vout and output current Iout respectively. Fig. 9 (a) and (b) shows the output voltage Vout and output current Iout of proposed 5-level topology respectively. It is shown that the levels of Vout are the same as in conventional topology with the same values of output voltage but with lower number of DC sources or split capacitors. From modes of operation, it is noticed that the current flows through 2 switches and 1 or 2 diodes in the proposed topology which is less than the conventional topology and this increases the

efficiency. Fig. 10 (a) and (b) shows the harmonic spectrum waveform of the output voltage Vout and output current Iout of proposed topology respectively.

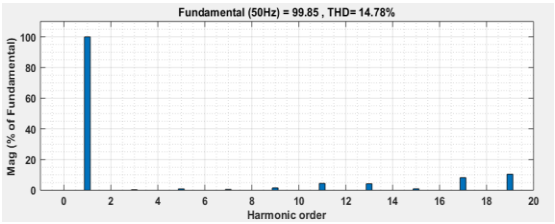


(a)

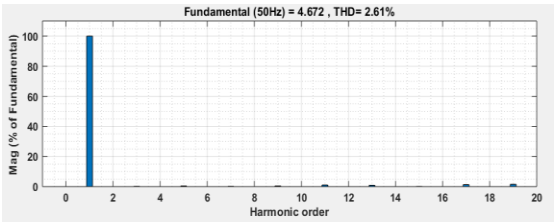


(b)

Fig. 7 Output voltage and current of conventional topology (a) Vout (b) Iout

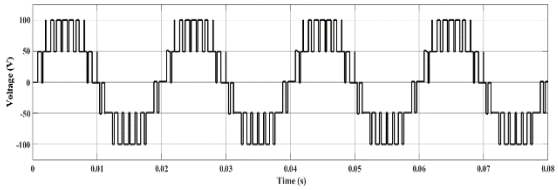


(a)

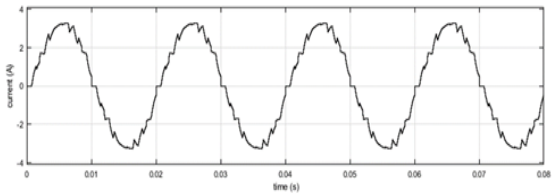


(b)

Fig. 8 Harmonic spectrum of (a) Vout (b) Iout of conventional topology.

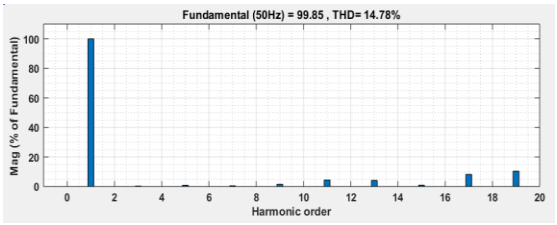


(a)

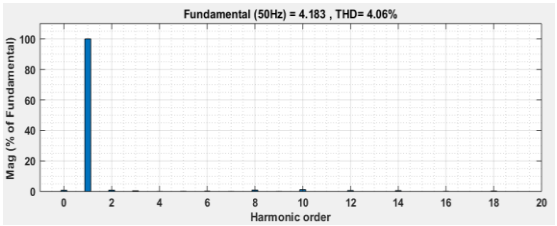


(b)

Fig. 9 Output voltage and current of proposed topology (a) Vout (b) Iout



(a)



(b)

Fig. 10 Harmonic spectrum of (a) Vout (b) Iout of proposed topology

4. Conclusions

This paper presents a new five-level inverter and compare it with conventional five-level NPC inverter. Results show that the proposed one has two main advantages over the conventional one. Firstly, the proposed topology utilizes only two DC sources instead of four DC sources in conventional one to produce the same levels of output voltage. Secondly, there are only two switches are turned on instead of four switches in every mode as in conventional topology and this can save in conduction losses.

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