# DSC-based Generation of Sinusoidal PWM Signals with the Least Number of Variables for Single-, Two- and Three-phase inverters

توليد الإشارات ذات النبضة المتغيرة بدالة جيبية وباستخدام متحكم الإشارات الرقمى بالحد الأدنى من المتغيرات لتطبيقات العاكس احادى وثنائى وثلاثى الأوجه

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يعتبر الآن العاكس هو العمود الفقري لكثير من الإستخدامات مثل مغيرات السرعة ومصادر القدرة الغير قابلة للإنقطاع وكذلك مرشحات القدرة الفعالة. فى الماضى كان التحكم فى العاكس يتم من خلال دوائر غطية والآن وبفضل المميزات المتعددة للمتحكمات الرقمية أصبحت هى المفضلة. وفى هذه الورقة البحثية يتم عرض طرق تنفيذ وتوليد الإشارات ذات النبضة المتغيرة بدالة جيبية حقيقية وباستخدام متحكم الإشارات الرقمي نظريا وعمليا وذلك للحد الأدنى من المتغيرات . والفكر المقترح يمكن استخدامه للعاكس سواء الأحادي أو الثنائي أو الثلاثي الأوجه بجميع أوجه التشغيل : أحادى أو ثنائي القطبية. وقد تم عمل دراسة للمحاكاة والتنفيذ العملي للخوارزم المقترح والذى أثبت فاعليته من حيث عدم الحاجة إلى دوائر غطية خارجية أو تخزين الموجة، مع إمكانية التعديل ليناسب أى عدد من الأوجه مع سهولة التحكم فقط فى متغير واحد وهو التردد المطلوب .

*Abstract* - **Inverters are the backbone of many applications such as adjustable speed drives (ASD), uninterruptible power supplies (UPS) and active power filters (APF). Although they have traditionally been controlled with analog circuits, digital control of inverters is now preferred. This paper covers theoretical and experimental aspects related to the implementation of a Digital Signal Controller (DSC)-based true Sinusoidal Pulse Width (SPWM) signals with the minimum number of variables. The technique is applied for single- , two- and three-phase inverters covering both bipolar and unipolar modes of operation. A simulation analysis is also carried out, then the resultant experimental and simulated waveforms were verified, showing the proposed algorithm advantages of no need for external analog circuits, no storing of wave patterns, flexible adaptation with any inverter number of phases, and only single variable is manipulated, that is the fundamental frequency ($f_m$).**

*Keywords:- Digital processing, Pulse width modulation, Power electronics, Inverter.*

## I. INTRODUCTION

**Techniques for producing controlled output voltage and frequency in pulse-width modulated (PWM) inverters have been known to exist in several prior works [1,2]. In the early days, the carrier-modulated PWM techniques based on analog circuitry, such as the triangular wave comparison type PWM, were very popular. Recently, the digital generation of PWM is far preferred as it is more accurate, reliable and less sensitive to noise. Microcomputer based techniques using preprogrammed PWM patterns have also been utilized. In these techniques, the PWM patterns, stored in an EPROM or in a look-up table in the RAM, are generated by computing the switching edges that satisfy specified performance requirements such as controlling the fundamental component and eliminating certain harmonics [2, 3-5]. Since sinusoidal PWM allowed the elimination of unwanted voltage harmonics from the output voltages, it was adopted as the major PWM technique in most applications, such as UPS and especially in ASD systems. One of the most popular methods to drive the induction motor is the constant-flux control, also called constant (V/f) control. The technique is based on keeping the flux constant by keeping the ratio between the stator voltage and frequency constant, thus resulting good drive characteristics with constant maximum torque and smoothly shifted torque-speed characteristics. The constant V/f control technique is best achieved with sinusoidal PWM as it provides separate control on both voltage magnitude and frequency. With semiconductors advances, digital signal processors and microcontrollers were invented and introduced to the market with task-oriented optimum designs and affordable prices. Still, the method of producing PWM was based on look-up tables where the modulating signal is stored in an array [4-16].**

**This paper discusses a method for generating gate signals suitable for single- , two- and three-phase sinusoidal pulse-width modulated inverter used in adjustable speed drives. For this particular application, the algorithm is designed to require only the least number of variables. In the case of single- and three-phase systems, only one variable is needed, that is the fundamental frequency, whereas, in two-phase systems, the fundamental frequency along with the phase-shift**

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may be required. Simulation – using MATLAB/SIMULINK – and experimental verification – with Texas Instrument's TMS320LF2812 DSC – of the technique are presented for each case. Using FFT, the frequency spectrum of output waveforms in both cases is shown. The SPWM strategy implemented in this work is based on comparing a triangular carrier with frequency $f_c$ and a reference discrete sinusoidal waveform with the required fundamental frequency $f_m$.

## II. INVERTER OPERATION MODES

Since the inverter is required to produce a sinusoidal output voltage waveform with controllable magnitude and frequency, a sinusoidal control signal (modulating signal) at the desired frequency is compared with a triangular waveform (carrier signal). The frequency of the triangular waveform ($f_c$) sets the inverter switching frequency and is kept constant along with its peak $V_{tri}$. The control signal $v_{control}$ is used to modulate the switch duty ratio and has a frequency ($f_m$), which is the desired fundamental frequency of the inverter voltage output. The amplitude modulation ratio ($m_a$) is defined as:

$$m_a = V_{control} / V_{tri} \quad (1)$$

Where $V_{control}$ and $V_{tri}$ are the peak values of the control and carrier signals.

The frequency modulation ratio ($m_f$) is defined as: $m_f = f_c / f_m$ (2)

In the 1-ph half-bridge inverter of figure1-a, the switches $Q_1$ and $Q_2$ are controlled based on the comparison of $v_{control}$ and $v_{tri}$, and the following output voltage results,

If $v_{control} > v_{tri}$, then $Q_1$ is on and $Q_2$ is off, thus $V_{AN} = + V_{dc} / 2$

else if $v_{control} < v_{tri}$, then $Q_2$ is on and $Q_1$ is off, thus $V_{AN} = - V_{dc} / 2$ (3)

The output voltage $V_{AN}$ is bipolar and varies from $(+V_{dc}/2)$ to $(-V_{dc}/2)$.

Whereas, for the full-bridge inverter shown in figure1-b, diagonally opposite switches ($Q_1$, $Q_4$) and ($Q_2$, $Q_3$) are connected as switch pairs 1 and 2, respectively. In this case, the output voltage waveform of leg A ($v_{AN}$) is identical to the output of the half-bridge inverter, which is determined by comparing $v_{control}$ and $v_{tri}$. The output of inverter leg B ($v_{BN}$) is the negative version of the leg A output ($v_{AN}$). The inverter output is then:

$$v_o = v_{AB} = v_{AN} - v_{BN} = 2 * v_{AN} = \pm V_{dc} \quad (4)$$

The output voltage $v_O$, and its corresponding sinusoidal RL load current are shown in figure 2-left. As the output switches between two values: $-V_{dc}$ and $+V_{dc}$, this type of switching is called bipolar voltage switching. The peak of the fundamental-frequency component in the output voltage is:-

$V_{O1} = m_a * V_{dc}$ for $m_a < 1.0$, and

$V_{dc} < V_{O1} < 4V_{dc}/\pi$ for $ma > 1.0$ (5)

If the switches in the two legs of the full-bridge inverter are not switched simultaneously, rather the legs A and B are controlled separately by comparing $v_{tri}$ with $v_{control}$ and $-v_{control}$ respectively, as shown in figure 2-right, the comparison of $v_{control}$ with the triangular waveform results in the following logic signals to control the switches in leg A:

$v_{control} > v_{tri}$: $Q_1$ is on and $v_{AN} = V_{dc}$

$v_{control} < v_{tri}$: $Q_2$ is on and $v_{AN} = 0$ (6)

For controlling the leg B switches, $-v_{control}$ (complementary value in digital systems) is compared with the same triangular waveform, which yields to:

$(-v_{control}) > v_{tri}$: $Q_3$ is on and $v_{BN} = V_{dc}$

$(-v_{control}) < v_{tri}$: $Q_4$ is on and $v_{BN} = 0$ (7)

The inverter output is then:

$$v_O = v_{AN} - v_{BN} = v_{AB} \quad (8)$$

Since the output voltage changes between zero and $+V_{dc}$ or between zero and $-V_{dc}$ voltage levels, this PWM scheme is called unipolar voltage-switching. It has the advantage of doubling the switching frequency; also, the voltage jumps at each switching are reduced to $V_{dc}$, rather than $2V_{dc}$ in the bipolar scheme, with less harmonic distortion. As shown in figure 2-c, bipolar mode has harmonic components around $n*f_m*m_f$, while unipolar modes has harmonic components around $2n*f_m*m_f$. The same principle can be applied to leg A and leg B of figure 1-b, but with variable phase-shifts ranging from $0^0$ to $180^0$ between the two control signals, thus obtaining two-phase SPWM voltages with variable phase-shift. Adding leg C to the inverter as shown on figure 1-c results in three-phase inverter, where three identical sinusoidal control signals with 0, $120^0$ and $240^0$ phase-shift respectively are introduced to generate 3-ph SPWM output voltages.

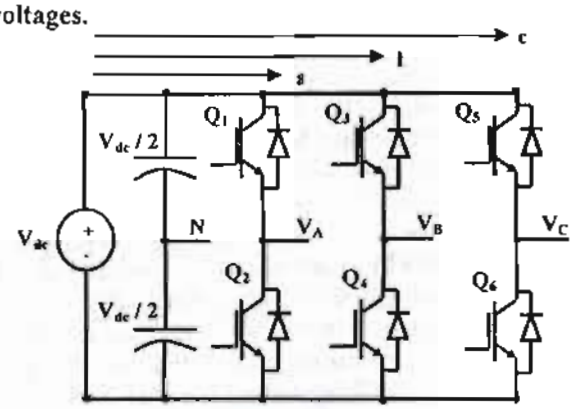
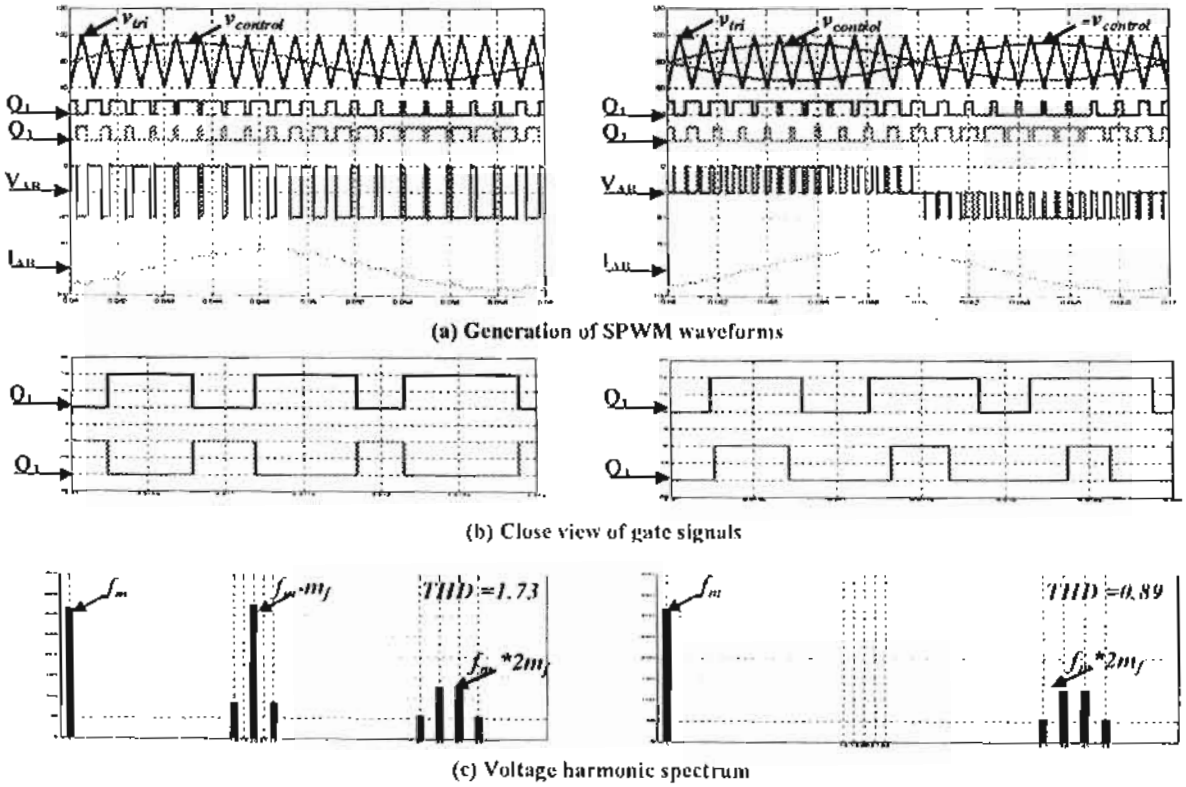



Figure 1: Inverters: a- Half-bridge, b- Full-bridge, and c- Three-phase.

## III. DIGITAL IMPLEMENTATION OF SPWM

*A - Stored PWM pattern*

A fairly straightforward method is to use an EPROM to directly store the PWM switching pattern. Each pattern is sequentially fed into the gate drive circuits, which will switch the transistors accordingly. The data for producing one cycle of the power waveform is divided into $2^n$ partitions and stored in the EPROM memory locations. For an inverter having Q number of switches, $2^n * Q$ bits of memory are required.




(a) Generation of SPWM waveforms

(b) Close view of gate signals




(c) Voltage harmonic spectrum

Figure 2: Simulation analysis of the single phase inverter to generate SPWM
Left: Bipolar mode Right: Unipolar mode

A counter, designed to count from 0 to $2^{n-1}$ in a repetitive cycle, is used as the address input to retrieve information from the EPROM. An external voltage signal can be used to control the oscillator frequency and hence the sampling frequency of the inverter. Major drawbacks are the magnitude of the output voltage is uncontrollable; hence this system cannot be used in constant flux (V to f) adjustable speed drives and the accuracy of the output is proportional to the memory size [3].

*B – Stored digital sine wave:*

*1 - Microprocessor (μP) Based system:*

A microprocessor with two digital counters/timers generating the addresses for two lookup tables: one for the triangular function, another for supplying the digital per-unit sine wave, whose frequency can vary. One multiplier for the modulation index and one hysterisis comparator must also be included. External analog to digital circuit for inputs entry and dead-band circuits for switches protection must be included, which makes the complete circuit comparatively big and less reliable [2].

*2 – Microcontroller (μC) based systems:*

Nowadays, with recent advances in embedded systems technology, there are many families of microcontrollers that include ADCs and PWM generators on chip. Among which are PIC, ATMEL and MOTOROLA families. The PWM generation unit contains programmable timers/counters with continuous-up or continuous-up/down modes to generate digital saw-tooth or triangular carrier waves respectively, which operates as carrier waves with frequency $f_c$, to produce asymmetric and symmetric PWM waveforms respectively. But with clock speeds as low as 16 MHz, the sine wave is still stored in a digital, fixed-point form in a look-up table. The instantaneous value of the sine wave is changed by simple multiplication by the control signal, while the modulating frequency $f_m$ is altered by changing the speed of reading the

sine wave values from the look up table. Still the accuracy of the output is a matter of concern since it is dependent on the size of the look-up table where the sine wave is stored. Also, these systems are not equipped with dead-band timers for edge delays, which is a matter that should be accounted for in the program or could be built as an external hardware for each switch. [3-5].

*3 – Digital signal processor (DSP) based systems:*

DSP manufacturers produced special purpose chips fully equipped with embedded units such as ADC, PWM generators, pulse encoders captures and dead-band timers, that makes them an optimal choice for power electronics control and ASD systems. Among which are: the Texas Instrument TMS320LF24xx family and the Motorola DSP56F805. Both have a 16bit fixed-point DSP core and a speed range of up to 40 MIPS, which is a limitation.

A method of generating SPWM was proposed, where the sine wave is still stored in its digital per-unit form in a look up table but the frequency of the modulation is controlled with some accuracy. The method is based on a module-mathematical operation, where the remainder is kept and the overflow is disregarded. A 16-bit counter is used to determine the location of the next sine wave value and a step value is added every time a new value from the sine table is to be loaded. By changing the value of the step, one can accurately control the frequency of the sine wave. One drawback is that the frequency that the PWM signal will be modulated is proportional to the step size (memory) and inversely proportional to the size of the counter register and the period at which the routine is accessed. [9-11].

*C - Taking advantage of digital signal controller (DSC) Technology*

Digital Signal Controllers (DSC) combine the traditional strengths of Digital Signal Processors (DSP) with that of Microcontrollers (MCU) into a single unified device. Together, the DSP's mathematical performance and data throughput and the MCU's low-cost integration and ease of use, form a powerful single-chip solution ideal for many embedded applications. With up to 150 Mega Instruction per Second (MIPS) of 32-bit DSP processing capability, the Texas Instrument TMS320LF2812 platform is the performance leader in the DSC market, It provides single-cycle 32x32 multiply/accumulate (MAC) and instruction execution, powerful addressing modes, shifters and integrated real-time emulation. [17, 18].

The TMS320LF2812 controller platform also features flexible control capabilities including fast interrupt response with automatic context save and restore; ultra-high speed-integrated ADCs; and powerful high-resolution PWM generators. For power electronics control, high-resolution PWM generators provide ultrahigh precision — 16 bits at 100 kHz or 12 bits at 1 MHz with programmable dead-time and phase or duty-cycle control. Two Pulse Width Modulator modules are included. These modules each incorporate three complementary, individually programmable PWM signal outputs (each module is also capable of supporting six independent PWM functions for a total of 12 PWM outputs) to enhance load control functionality. The device is capable of controlling either two three-phase inverters or six single-phase inverters simultaneously. Complementary operation permits programmable dead-time insertion, distortion correction, and separate top and bottom output polarity control. In this work, all the traditional analog circuitry used to generate true SPWM has been replaced by digital schemes, embedded in the program. This allows for an extremely reliable and cost-effective solution.

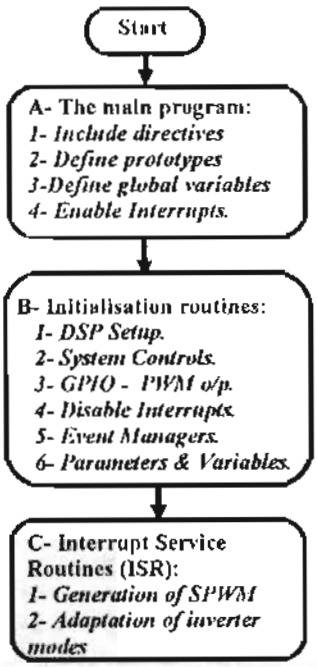



Figure 3: Simplified flow chart of the proposed program.

## IV. THE PROPOSED DIGITAL SIGNAL CONTROLLER (DSC) SOFTWARE

The digital signal controller software consists of two main units, the Compiler/Debugger Software Package, and the main program. The Code Composer Studio™ software is supplied with the

DSP and used as a compiler and debugger in this implementation [19]. The simplified flowchart of the algorithm is shown in figure 3, and can be described in some details as follows:-

*A – The Main program*

The main program, written in C, includes directives (header files), defines various prototypes, defines global variables, and executes initialising and running routines.

*B – Initialisation Routines*

The first stage after including header files, defining prototypes and global variables is calling six initialising routines, which are in details:

*1 - The DSP setup:* this includes initialising system control registers which adjust the internal PLL (Phase locked loop) and internal clock multiplier for an operating clock of 150 MHz ($f_{clk}$), disable the watchdog timer, set up the external memory interface, and enable pre-scaled clock input for chosen peripherals. Next, the GPIO (general purpose input/output registers) are set to enable PWM outputs on associated pins.

*2 - Interrupt vectors and flags:* all flags are cleared and CPU interrupts are disabled.

*3 - Initializing the Interrupt Service Routines (ISR):* only the ones that are used in this project are initialised, which are: timer one and three period interrupts.

*4 - Event manager initialisation:* this involves setting up the EVM control and action registers, timers' counters, periods, compare registers and dead band timers. In details, the event manager initialisation does the following:

*i - Sets up EVM control and action registers:*

Enable compare action, toggle PWM outputs in case of compare match, and determine which outputs are active-high and which are active-low. On period match reloading of compare register, thus updates the output pulse width.

*ii - Sets up timer/counter registers:*

Since the input clock to the timers is $f_{clk}$ = 150 MHz and it is required to produce a carrier signal of frequency $f_c$ = 5 kHz, then the total number of counts in one period of carrier signal is: Carrier signal span = $f_{clk}/f_c$ = 30,000 counts (9)

Since for symmetrical PWM, the carrier wave should be triangular rather than saw- tooth, the timers' period registers need only be half the previous value to produce the required signal span, hence:

T1&T3 period registers = Carrier signal span / 2
= 15,000 counts = 0x3A98 (10)

Since this DSP is based on fixed point arithmetic, then the datum of the signal that is considered as analogue zero is the mid-range value that is 0x1D4C. Thus, the initialisation sets up counters one and three continuous up/down and load their period registers with 0x3A98 counts, thus producing a triangular wave with fixed frequency of 5 kHz. Also restores timers one and three counters values to mid-range (0x1D4C), which is equivalent to zero. Similarly, all compare registers are set to mid-range value to produce zero voltage on the output.

*iii - Sets up dead band timers:*

To guarantee a safe switching for series IGBTs under highly inductive loading, a dead band period must be introduced between inverted gate signals to prevent any short-circuit occurrence. Hence, ($Q_1$&$Q_3$), and ($Q_2$&$Q_4$) should always be zero. According to SIMENS IGBT data sheet, the minimum dead band time required for safe operation of series IGBT is 600 ns, thus all the dead band timers were enabled and loaded with a specific count that causes a time separation of 2 μs between inverted PWM signals that feed series IGBTs.

*5 - Initialising parameters and variables:* this involves setting the values of the system parameters such as the maximum peak voltage, the V/f ratio, and their corresponding digital values for fixed-point calculations. Also, setting the value of some variables that can be changed later via the user or during operation, such as modulating signal frequency, the maximum value of sample counter and – upon need - the phase-shift between modulating waves. In program description language, the initializing routine will be:

```
// Enter the modulating / output frequency
f = 50
// Enter the phase shift, if applicable
Pshiftr = (-90 * 3.14169265) / 180
// the sampling frequency
fs = 5000
// the maximum value of sample counter
Kmax = fs / f
// the digital peak value for max. peak voltage of
220*sqrt(2)
Amp_max = 0x1D4C.
// V to F ratio
Vtof = Amp_max / fmax;
// calculate amplitude based on frequency and V/f
ratio
Amp = Vtof * f
```

*6- Interrupts should be in turn enabled:* these interrupt signals are responsible for calling the corresponding ISR: Interrupt Service Routines. For single- and three-phase inverters, only one timer/counter with its compare/PWM unit is required, whereas for two-phase inverters, two timers/counters are a must.

*C – Interrupt Service Routines*

*1 – Generation of the SPWM*

In order to obtain a symmetrical PWM, regular sampling of the sine wave is done with the carrier frequency [12], i.e. when the continuous up/down counter reaches its maximum number of counts, hence $f_s = f_c$. Thus, the Interrupt Service Routine (ISR) is called on period match and the frequency of this interrupt is set to be the carrier frequency ($f_c$) 5kHz. The continuous time base must be converted to a discrete one in order to calculate the angle at each sample then to calculate the sine of such angle, then: $T = KT_s = KT_c$ (11)

$sin\ ( 2\pi * f_m * t ) = sin\ ( 2\pi * f_m * KT_c )$ (12)

where $f_m$ is the modulating frequency, $T_c$ is the sampling time, and K is the sample counter. Equation (12) can be rewritten as:

$sin\ ( 2\pi * K * (f_m / f_c) ) = sin\ ( 2\pi * K / m_f)$ (13)

where $m_f$ is the frequency modulation index.

The maximum value of the sample counter is when the angle reaches $2\pi$, hence

$2\pi * K_{max} / m_f = 2\pi$, thus, $K_{max} = m_f = f_c / f_m$ (14)

After which the sample counter should be zeroed for the new modulating cycle. Every sample, the sample counter is increased then the new angle and its sine function are calculated. Based on the known V/f ratio, the peak value ($V_{pk}$) is calculated from:

$V_{pk} = (V/f\ ratio) * f$ (15)

then multiplied by the sine function to produce the modulating value in this sample.

$mod1 = V_{pk} * sin\ ( 2\pi * K / m_f)$ (16)

Next, the outcome is offset by the mid-value, which corresponds to zero, to calculate the fixed-point digital value.

$mod1\_FP = mod1 + 0x1D4C$ (17)

Finally, the latter is sent to a compare register in the PWM generation unit to produce bipolar SPWM gate signals.

In unipolar mode, two modulating signals are required: the sine wave and its inverse. In fixed-point digital system the modulating value is inverted by taking its complement, that is:

$mod2\_FP = 0x3A98 - mod1\_FP$ (18)

then sent to another compare register, both compare values produce gating signals for unipolar mode.

Even for phase-shifted modulating signals, the previous calculations still hold. Thus, for a phase-shift ($\Phi$), we have:

$sin\ ((2\pi * f_m * t \pm \Phi)) = sin\ ((2\pi * f_m * KTc) \pm \Phi)$

$= sin\ ((2\pi * K / m_f) \pm \Phi)$ (19)

The ISR in program description language:

```
// incrementing the sample counter
K = K + 1
// reset the sample counter to zero if it reaches its
maximum
if (K > (Kmax-1)) then (K = 0)
// calculate the angle in discrete form
theta1 = (2*3.14169265*f*K) / fs
// calculate its sine value
x1 = sin(theta1)
// calculate the magnitude of the modulating sine
wave
mod1 = Amp * x1
// scale it from 0x0000 to 0x3A98 to match the
counter
mod1_FP = mod1 + 0x1D4C
// For unipolar mode, the inverse modulating
signal is:
mod2_FP = 0x3A98 - mod1_FP
// update the compare register value
CMPR1 = mod1_FP
CMPR2 = mod2_FP
// finally, enable more interrupts from this timer
EvaRegs.EVAIMRA.bit.T1PINT = 1;
```

*2- Adaptation according to inverter operation modes:*

In two-phase bipolar mode, the phase-shifted modulating signals are calculated and sent to two compare registers, thus, only one timer unit is needed for such application. Whereas, in unipolar mode, each modulating signal requires two compare registers, hence, using two timer units is a must.

While, in three-phase systems, it is known beforehand that the phase shift between the modulating signals is 120 degrees and the output line voltages are unipolar. Thus, the three modulating signals are digitally calculated, then sent to three compare registers in one timer-unit. In all systems, upon match between the counter and the compare register, the output toggles its state. This happens twice in continuous up/down counting, which finally produces SPWM signals.

## V. EXPERIMENTAL RESULTS OF THE PROPOSED ALGORITHM

Since in a conventional induction machine the operating frequency is 50, this value will be taken as the maximum modulating frequency having the largest amplitude to obtain a constant V/f ratio through all the following experimental tests of the proposed algorithm, while carrier frequency is fixed at $f_c$ of 5 kHz and each lower transistor has a complemented gate signal of the upper transistor with 2 μs dead time interval.

*A - Single-Phase Inverters*

In this case, only one variable need to be manipulated, that is the frequency. All other variables are calculated correspondingly. Two SPWM modes of operation are covered; the bipolar, shown in figure 4, and the unipolar

shown in figure 5. For 50 Hz, wide positive and negative pulses represent the fundamental positive and negative peak value with time span between cursors is 10 msec; while at 40 Hz, output voltage waveforms have no wide pulses since the peak voltage is less than 1 p.u to keep the V/f ratio constant and the time span in this case is around 12.5 msec. It can be seen the practical results of the proposed algorithm depicted trough figures 4 and 5 well correlated with the corresponding simulated results obtained in figure 2, showing the effectiveness of the proposed algorithm.

*B - Two-Phase Inverters*

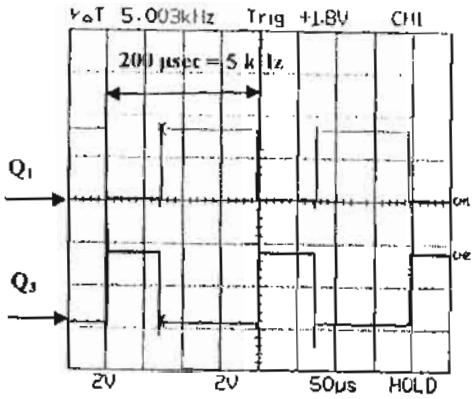
They may be used in driving two-phase machines. Both the frequency and phase-shift between phases could be required to determine the SPWM signals. All other variables are calculated correspondingly. Bipolar and unipolar output voltage modes of operation are attainable and the output voltages will be the same as the ones shown in previous output voltage figures. To validate the work, various phase shifts between gate signals producing SPWM waves with the same carrier frequency, taken as 50 Hz for clarity, are demonstrated. Phase shifts of 30°, 45°, 60°, and 90° are shown in figure 6-a, b, c, and d respectively, with cursors showing the phase shift between peaks degrees.

*C - Three-Phase Inverters*

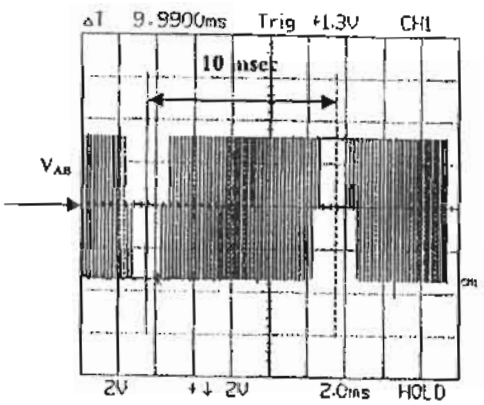
They are most used in ASD, APF and UPS systems. Still only the fundamental frequency is required to generate SPWM signals, as the phase-shift is constant at 120° electrical. All other variables are calculated correspondingly through the program. The phase voltages are bipolar, while the line voltages are unipolar. Figure 7a and 7b, show the gate signals at $f_m$ = 50 and 40 Hz respectively.

## VI. CONCLUSIONS

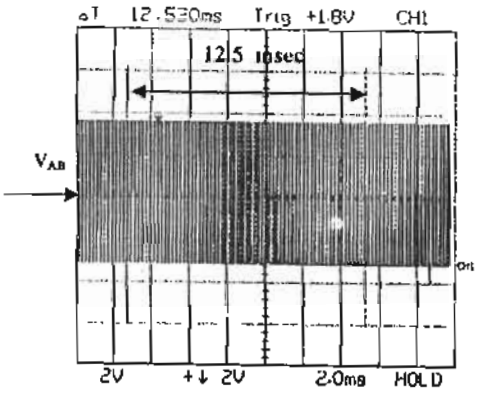
Based on the obtained simulation and experimental results, digital signal controllers (DSC) can be considered as a perfect tool for real time implementation for power electronics applications. The proposed algorithm of modulating signal generation by calculating the true sine value in its discrete form has been proven successful with the advantages of:- All features are implemented through software, so no need for external analog circuitry, no storing of wave patterns, hence no limitation of memory size, flexible adaptation with any inverter number of phases, thus can be implemented in different inverter based applications, and only single variable is manipulated ($f_c$), while other variables are then calculated, providing simple and powerful inverter final control loop to be combined with other cascaded control loops.



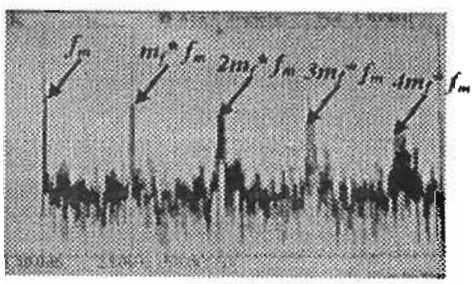

(a) Gate signals




(b) Voltage waveform at $f_m$ = 50 Hz, $V_{AB\,peak} = V_{dc}$

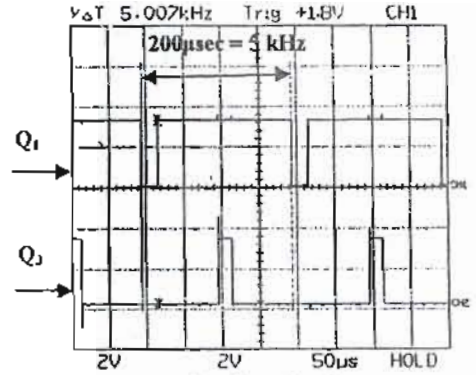



(c) Voltage waveform at $f_m$ = 40 Hz, $V_{AB\,peak} = 0.8V_{dc}$

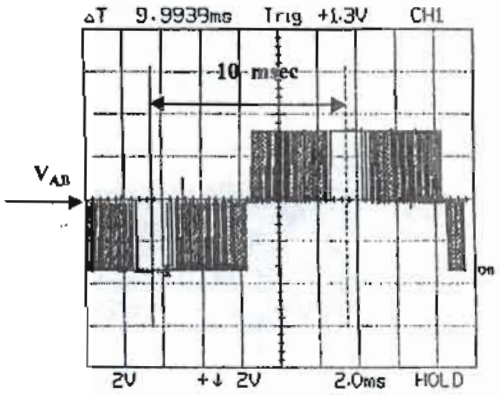



(d) Voltage harmonic spectrum

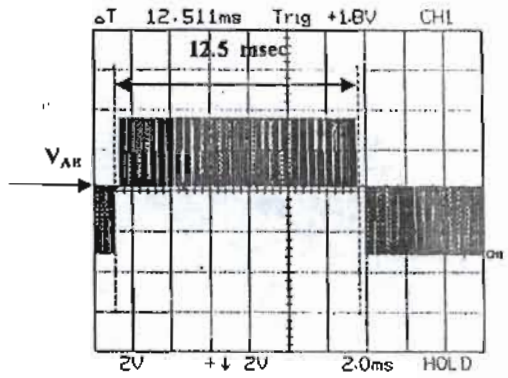
Figure 4: Experimental results of single phase inverter with bipolar mode of operation



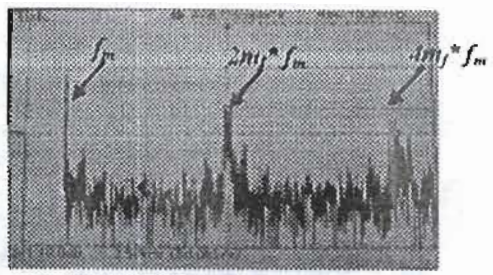

(a) Gate signals




(b) Voltage waveform at $f_m = 50$ Hz, $V_{AB\,peak} = V_{dc}$




(c) Voltage waveform at $f_m = 40$ Hz, $V_{AB\,peak} = 0.8V_{dc}$




(d) Voltage harmonic spectrum

Figure 5: Experimental results of single phase inverter with unipolar mode of operation

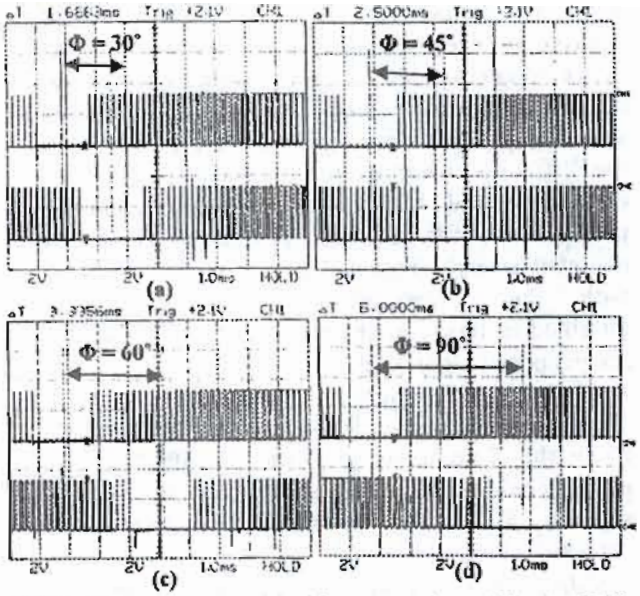
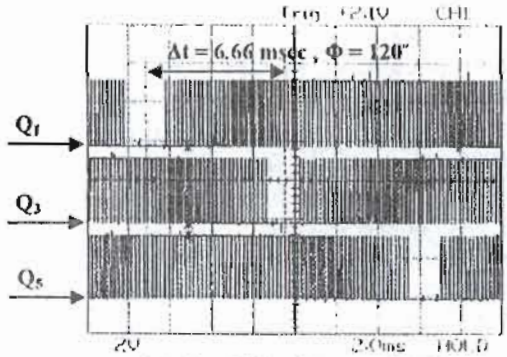
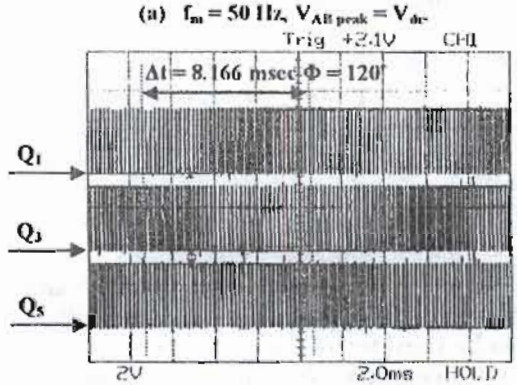



Figure 6: Two-phase SPWM with various phase-shifts $f_m$ =50 Hz.




(a) $f_m = 50$ Hz, $V_{AB\,peak} = V_{dc}$




(b) $f_m = 40$ Hz, $V_{AB\,peak} = 0.8V_{dc}$

Figure 7: Gate signals for 3-phase inverter to get SPWM voltages at fixed (V/f) ratio.

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